IN THE CLAIMS

Please cancel claims 1-3, 6, 14-15, and 18 and amend claims 4, 7, 11, 16, and 19 as follows:

1. (Canceled) In a data processing system having a processor responsively coupled to a store-in cache memory which is responsively coupled to a lower level memory, the improvement comprising:

a. a read-only level one instruction cache memory directly coupled to said processor;

b. a store-through level one operand cache memory directly coupled to said processor;

c. wherein said processor is responsively coupled to said store-in cache memory via said read-only level one instruction cache memory and via said store-through level one operand cache memory; and

d. a flush buffer directly coupled to said store-in cache memory and said lower level memory.

2. (Canceled) A data processing system according to claim 1 further comprising a tag memory responsively coupled to said store-in cache memory which indicates whether a particular

location within said store-in memory has been modified by said processor.

3. (Canceled) A data processing system according to claim 2 further comprising a logic circuit which loads said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location within said store-in memory has been modified by said processor.

4. (Currently Amended) In a data processing system having a processor responsively coupled to a store-in cache memory which is responsively coupled to a lower level memory, the improvement comprising:

a. a read-only level one instruction cache memory directly coupled to said processor;

b. a store-through level one operand cache memory directly coupled to said processor;

c. wherein said processor is responsively coupled to said store-in cache memory via said read-only level one instruction cache memory and via said store-through level one operand cache memory; d. a flush buffer directly coupled to said store-in cache memory and said lower level memory;

e. a tag memory responsively coupled to said store-in cache memory which indicates whether a particular location within said store-in memory has been modified by said processor;

f. a logic circuit which loads said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location within said store-in memory has been modified by said processor; and

g. ~~according to claim 3~~ wherein said flush buffer further comprises a first flush buffer store having a first input responsively coupled to said store-in cache memory and a first output directly coupled to said lower level memory and a second flush buffer store having a second input responsively coupled to said store-in cache memory and a second output directly coupled to said lower level memory.

5. (Original) A data processing system according to claim 4 further comprising a temporary register responsively coupled to said store-in cache memory, said first flush buffer store, and said second flush buffer store which routes said data from said particular location to an available one of said first flush buffer store and said second flush buffer store.

6. (Canceled) A data processing system comprising:

a. A processor;

b. A level one store-through cache memory having a read-only instruction portion and an operand portion directly coupled to said processor;

c. A store-in cache memory responsively coupled to said processor via said read-only instruction portion and said operand portion of said level one store-through cache memory;

d. A lower level memory responsively coupled to said store-in cache memory; and

e. A flush buffer directly coupled to said store-in cache memory and said lower level memory.

7. (Currently Amended) A data processing system ~~according to claim 6~~ comprising:

a. A processor;

b. A level one store-through cache memory having a read-only instruction portion and an operand portion directly coupled to said processor;

c. A store-in cache memory responsively coupled to said processor via said read-only instruction portion and said operand portion of said level one store-through cache memory;

d. A lower level memory responsively coupled to said store-in cache memory;

e. A flush buffer directly coupled to said store-in cache memory and said lower level memory; and

f. wherein said flush buffer further comprises a first flush buffer store having a first input responsively coupled to said store-in cache memory and a first output directly coupled to said lower level memory and a second flush buffer store having a second input responsively coupled to said store-in cache memory and a second output directly coupled to said lower level memory.

8. (Original) A data processing system according to claim 7 further comprising:

a. A temporary register responsively coupled to said store-in cache memory, said first flush buffer store, and said second flush buffer store.

9. (Original) A data processing system according to claim 8 further comprising:

a. A tag memory responsively coupled to said store-in cache memory for indicating whether a particular location has been modified by said processor.

10. (Previously presented) A data processing system according to claim 9 further comprising:

a. A logic circuit responsively coupled to said tag memory, said store-in cache memory, and said temporary register which routes data from said particular location from said store-in cache memory to said temporary register when said indication is that said particular location has been modified by said processor.

11. (Currently Amended) A method of flushing a store-in cache memory responsively coupled to a level one store-through operand cache memory comprising:

a. Receiving a data request at said store-in cache memory from said level one store-through operand cache memory;

b. Searching said store-in cache memory in response to said data request;

c. Experiencing a cache miss in response to said searching step;

d. Selecting a particular location within said store-in cache memory to be flushed; ~~and~~

e. Choosing a one of two flush buffer stores wherein each of said two flush buffer stores has a separate and independent input responsively coupled to said store-in cache memory and a separate and independent output responsively coupled to lower level memory;

f. Transferring data from said particular location to ~~a~~ said one of two flush buffer stores chosen by said choosing step through its separate and independent input; and

g. Flushing said data from said one of two flush buffer stores chosen by said choosing step to said lower level memory via its separate and independent output.

12. (Original) A method according to claim 11 further comprising:

a. Determining whether data within said particular location was modified by a processor.

13. (Original) A method according to claim 12 further comprising:

a. Inhibiting said transferring step if said determining step determines that said data within said particular location was not modified by said processor.

14. (Canceled) A method according to claim 13 wherein said transferring step further comprises routing said data to the available one of a first flush buffer store and a second flush buffer store.

15. (Canceled) A method according to claim 14 further comprising:

a. Rewriting said data to a lower level memory following said transferring step.

16. (Currently Amended) An apparatus comprising:

a. Means for executing program instructions;

b. Means responsively coupled to said executing means for handling operands in a store-through level one cache memory;

c. Means responsively coupled to said handling means for caching data on a store-in basis; ~~and~~

d. Means responsively coupled to said data caching means for providing lower level storage;

e. Means directly coupled to said caching means for buffering data from said caching means to be flushed having a first storing with a first input directly coupled to said data caching means and a first output directly coupled to said providing means and having a second storing means with a second input directly coupled to said data caching means and a second output directly coupled to said data caching means.

17. (Original) An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said caching means for selecting said data to be flushed.

18. (Canceled) An apparatus according to claim 17 wherein said buffering means further comprises a first means for storing having a first input and a first output and a second means for storing having a second input and a second output.

19. (Currently Amended) An apparatus according to claim ~~18~~ 17 further comprising:

a. Means responsively coupled to said first storing means and said second storing means for routing said data to the available one of said first storing means and said second storing means.

20. (Original) An apparatus according to claim 19 further comprising:

a. Means responsively coupled to said caching means for determining whether said data has been modified by said executing means; and

b. Means responsively coupled to said determining means and said buffering means for inhibiting transfer of data from said caching means to said buffering means if said determining means

determines that said data has not been modified by said executing means.